EXHIBIT 3

U.S. Patent No. 6,799,295 – ASUSTeK Computer Inc.

Claim 1

TurboCode LLC ("TurboCode") provides evidence of infringement of claim 1 of U.S. Patent No. 6,799,295 (hereinafter "the '295 patent") by ASUSTeK Computer Inc ("Asus" or "Defendant"). In support thereof, TurboCode provides the following claim charts.

"Accused Instrumentalities" as used herein refers to at least cellular telephones, tablet computers, and/or other devices with 3G and/or 4G/LTE capabilities and that comply with the 3G and/or 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications governing cellular wireless communications (e.g., TS 36.101-36.978, TS 26.071-26.999), and similar systems, products, and/or devices (including, but not limited to the Asus ZenFone 7 Pro). These claim charts demonstrate Asus's infringement, and provide notice of such infringement, by comparing each element of the asserted claims to corresponding components, aspects, and/or features of the Accused Instrumentalities. These claim charts are not intended to constitute an expert report on infringement. These claim charts include information provided by way of example, and not by way of limitation.

The analysis set forth below is based only upon information from publicly available resources regarding the Accused Instrumentalities, as Asus has not yet provided any non-public information. An analysis of Asus's (or other third parties') technical documentation and/or software source code may assist in fully identify all infringing features and functionality. Accordingly, TurboCode reserves the right to supplement this infringement analysis once such information is made available to TurboCode. Furthermore, TurboCode reserves the right to revise this infringement analysis, as appropriate, upon issuance of a court order construing any terms recited in the asserted claims.

Unless otherwise noted, TurboCode contends that Asus directly infringes the '295 patent in violation of 35 U.S.C. § 271(a) by selling, offering to sell, making, using, and/or importing the Accused Instrumentalities. The following exemplary analysis demonstrates that infringement. Unless otherwise noted, TurboCode further contends that the evidence below supports a finding of indirect infringement under 35 U.S.C. §§ 271(b) and/or (c), in conjunction with other evidence of liability under one or more of those subsections. Asus makes, uses, sells, imports, or offers for sale in the United States, or has made, used, sold, imported, or offered for sale in the past, without authority, or induces others to make, use, sell, import, or offer for sale in the United States, or has induced others to make, use, sell, import, or offer for sale in the past, without authority products, equipment, or services that infringe claim 1 of the '295 patent, including without limitation, the Accused Instrumentalities.

Unless otherwise noted, TurboCode believes and contends that each element of each claim asserted herein is literally met through Asus's provision of the Accused Instrumentalities. However, to the extent that Asus attempts to allege that any asserted claim element is not literally met, TurboCode believes and contends that such elements are met under the doctrine of equivalents. More specifically, in its investigation and analysis of the Infringing Instrumentalities, TurboCode did not identify any substantial differences between the elements of the patent claims and the corresponding features of the Accused Instrumentalities, as set forth herein. In each instance, the identified feature of the Accused Instrumentalities performs at least substantially the same function in substantially the same way to achieve substantially the same result as the corresponding claim element.

To the extent the chart of an asserted claim relies on evidence about certain specifically-identified Accused Instrumentalities, TurboCode asserts that, on information and belief, any similarly-functioning instrumentalities also infringes the charted claim. TurboCode reserves the right to amend

this infringement analysis based on other products made, used, sold, imported, or offered for sale by Asus. TurboCode also reserves the right to amend this infringement analysis by citing other claims of the '295 patent, not listed in the claim chart, that are infringed by the Accused Instrumentalities. TurboCode further reserves the right to amend this infringement analysis by adding, subtracting, or otherwise modifying content in the "Accused Instrumentalities" column of each chart.

CLAIM CHART
U.S. Patent No. 6,799,295

Claim 1	'295 Accused Instrumentalities
1. A baseband processing system for iteratively decoding data received on multiple data paths, the baseband processing system comprising:	To the extent the preamble is found to be a limitation, as discussed below, the '295 Accused Instrumentalities perform a method of iteratively decoding a plurality of sequences of received baseband signals. The '295 Accused Instrumentalities include products, devices, systems, and components of systems that comply with the 3G and/or 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications governing cellular wireless communications and that were or are designed, developed, tested, made, used, offered for sale, sold in the United States, imported into the United States, or that have a nexus to the United States, including for example and without limitation, the following:[1] • Fonepad, PadFone, ROG Phone, and Zenfone series smartphones, MeMO Pad, Nexus, VivoTab, and ZenPad series cellular-enabled tablets, AC1900, 4G-AC86U, 4G-N12 B1, 4G-AC53U, 4G-AC55U, and 4G-AC68U series modem routers, Asus Laptop (e.g., BR1100), Chromebook, ExpertBook, NovaGo, and Transformer series cellular-enabled laptops, and similar products, devices, systems, and components of systems that comply with the 3G and/or 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications governing cellular wireless communications (*e.g.*, TS 36.101-36.978, TS 26.071-26.999). **Direct Infringement** Asus has directly infringed and continues to directly infringe at least Claim 1 of the '295 Patent under 35 U.S.C. § 271(a) by making, using, offering to sell, selling, within the United States, or importing into the United States without authorization the '295 Accused Instrumentalities. This direct infringement is described hereinbelow. **Indirect Infringement** Asus has induced and continues to induce infringement by others of at least Claim 1 of the '295 Patent

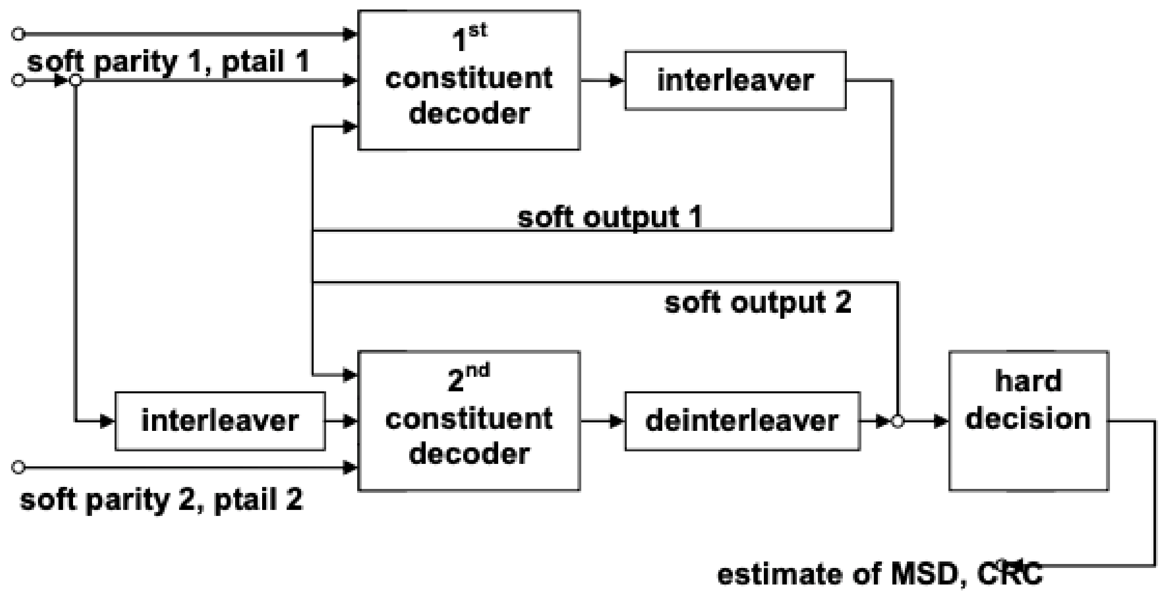
[1] The '295 Accused Instrumentalities are identified based on information currently available on Asus's website and other public information. TurboCode reserves the right to supplement, revise or otherwise amend this list, when additional model numbers are identified and new information becomes available during discovery.

	under 35 U.S.C. § 271(b) by encouraging its customers (including but not limited to manufacturers of the '295 Accused Instrumentalities or manufacturers using Asus's product designs for the '295 Accused Instrumentalities; manufacturers of computer products incorporating the '295 Accused Instrumentalities; and distributors, wholesalers, and retailers, and end users, to make, use, sell, offer to sell, and import in the United States without authorization the '295 Accused Instrumentalities of the underlying direct infringement. Asus has contributed to and continues to contribute to infringement by others of at least Claim 1 of the '295 Patent under 35 U.S.C. § 271(c) by selling, offering to sell, importing, and/or supplying in the United States without authority components of the products that infringe one or more claims of the '295 Patent, including but not limited to the '295 Accused Instrumentalities of the underlying direct infringement. Asus's ZenFone 7 Pro is a representative product because it performs iterative decoding in accordance with the 3G and/or 4G/LTE standards disclosed in the 3GPP Standard Specifications as do the '295 Accused Instrumentalities. For example, Asus's ZenFone 7 Pro complies with 3G and 4G/LTE as shown below:

	Network Standard GSM/GPRS/EDGE; WCDMA/HSPA+/DC-HSPA+; FDD-LTE; TD-LTE; 5G Sub 6 SA/NSA Data rate: Support EN-DC (5DL+FR1) FR1: DL up to 3.6 Gbps / UL 542 Mbps LTE 5CA: DL Cat 19 up to 1.8 Gbps / UL Cat 13 up to 150 Mbps DC-HSPA+: DL 42 Mbps / UL 5.76 Mbps 4x4 MIMO and CA with 4x4 MIMO support FDD-LTE (Bands 1, 2, 3,4, 5, 7, 8, 12, 17, 18, 19, 20, 26, 28, 29) TD-LTE (Bands 38, 39, 40, 41) WCDMA (Bands 1, 2, 3, 4, 5, 6, 8, 19) EDGE/GPRS/GSM (850, 900, 1800, 1900 MHz) 5G Non-Standalone (NSA): n1, n2, n3, n5, n7, n8, n12, n20, n28, n38, n77, n78 5G Standalone (SA): n77, n78 ASUS phone 5G/4G band compatibility varies by region, please check compatibility with local carriers. *See* Asus ZenFone 7 Pro Specification, *available at* https://www.asus.com/Mobile/Phones/All-series/ZenFone-7-Pro/techspec/. As another example, each accused instrumentality, including the ZenFone 7 Pro, includes a baseband processing system for iteratively decoding data received on multiple data paths. As another example, the ZenFone 7 Pro receive data over multiple data paths: "3GPP long term evolution (LTE) enhances the wireless communication standards UMTS and HSDPA towards higher throughput. A throughput of 150 Mbit/s is specified for LTE using 2×2 MIMO. For this, highly punctured Turbo codes with rates up to 0.95 are used for channel coding, which is a big challenge for decoder design. This paper investigates efficient decoder architectures for highly

	punctured LTE Turbo codes. We present a 150 Mbit/s 3GPP LTE Turbo code decoder, which is part of an industrial SDR multi-standard baseband processor chip." *See* M. May, T. Ilnseher, N. Wehn and W. Raab, *A 150Mbit/s 3GPP LTE Turbo code decoder*, Design, Automation & Test in Europe Conference & Exhibition, 2010, at 1420, *available at* https://past.date-conference.com/proceedings-archive/2010/DATE10/PDFFILES/10.4_5.pdf *See also* "LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception (3GPP TS 36.101 version 11.7.0 Release 11)," at 98, *available at* https://www.etsi.org/deliver/etsi_ts/136100_136199/136101/11.07.00_60/ts_136101v110700p.pdf ("3GPP TS 36.101) (LTE user equipment is expected to have at least two radio ports: "The requirements in Section 7[, 'Receiver characteristics,'] assume that the receiver is equipped with two Rx port as a baseline."). As another example, the ZenFone 7 Pro provide MIMO capability and Forward Error Correction (FEC) decoding: "1 Scope The present document describes a general description of the physical layer of the E-UTRA radio interface. The present document also describes the document structure of the 3GPP physical layer specifications, i.e. TS 36.200 series. The TS 36.200 series specifies the Uu and Un points for the 3G LTE mobile system, and defines the minimum level of specifications required for basic connections in terms of mutual connectivity and compatibility. … 4.1.2 Service provided to higher layers The physical layer offers data transport services to higher layers. The access to these services is through the use of a transport channel via the MAC sub-layer. The physical layer is expected to perform the following functions in order to provide the data transport service: … - FEC encoding/decoding of the transport channel … - Multiple Input Multiple Output (MIMO) antenna processing …

	4.2.1 Multiple Access … Transmission with multiple input and multiple output antennas (MIMO) are supported with configurations in the downlink with up to sixteen transmit antennas and eight receive antennas, which allow for multi-layer downlink transmissions with up to eight streams. Multi-layer uplink transmissions with up to four streams are supported with configurations in the uplink with up to four transmit antennas and four receive antennas. Multi-user MIMO, i.e., allocation of different streams to different users is supported in both UL and DL. *See* "LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); LTE physical layer; General description (3GPP TS 36.201 version 11.0.0 Release 11)," at 5-8, *available at* https://www.etsi.org/deliver/etsi_ts/136200_136299/136201/11.00.00_60/ts_136201v110000p.pdf (3GPP TS 36.201). As yet another example, in the ZenFone 7 Pro, Turbo decoding, which is form of FEC decoding, can be used when receiving turbo encoded data. Channel coding in LTE uses turbo coding: "4.2.3 Channel coding and interleaving The channel coding scheme for transport blocks in LTE is Turbo Coding with a coding rate of R=1/3, two 8-state constituent encoders and a contention-free quadratic permutation polynomial (QPP) turbo code internal interleaver. Trellis termination is used for the turbo coding. Before the turbo coding, transport blocks are segmented into byte aligned segments with a maximum information block size of 6144 bits. Error detection is supported by the use of 24 bit CRC. Further channel coding schemes for BCH and control information are specified in [3]." *See* 3GPP TS 36.201, at 9. As yet another example, in the ZenFone 7 Pro, turbo decoding involves iteratively decoding data, which may be received over multiple data paths: "A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively. The

	output of the first (upper decoder) feeds into the second to form a Turbo decoding iteration. Interleaver and deinterleaver blocks re-order data in this process." *See* ALTERA CORP., 3GPP LTE TURBO REFERENCE DESIGN, 7 (Jan. 2011), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf. An example turbo decoder is shown below:  **Figure 18: Turbo decoder** *See* "Digital cellular telecommunications system (Phase 2+); Universal Mobile Telecommunications System (UMTS); eCall data transfer; In-band modem solution; General description (3GPP TS 26.267 version 11.0.0 Release 11)," at 25, *available at* https://www.etsi.org/deliver/etsi_TS/126200_126299/126267/11.00.00_60/ts_126267v110000p.pdf ("3GPP TS 26.267").

at least one decoder adapted to receive the data received on one or more of the multiple data paths, wherein each decoder comprises: at least two soft decision decoders adapted to receive data associated with corresponding data paths, wherein the at least two soft decision decoders are serially coupled and have at least a first soft decision decoder and a last soft decision decoder, wherein the last soft decision decoder is adapted to output data for the serially coupled series of soft decision decoders;	The '295 Accused Instrumentalities include at least one decoder adapted to receive the data received on one or more of the multiple data paths, wherein each decoder comprises at least two soft decision decoders adapted to receive data associated with corresponding data paths, wherein the at least two soft decision decoders are serially coupled and have at least a first soft decision decoder and a last soft decision decoder, wherein the last soft decision decoder is adapted to output data for the serially coupled series of soft decision decoders. For example, the representative product, ZenFone 7 Pro, includes at least one such decoder adapted to receive the data received on one or more of the multiple data paths. An example decoder is a turbo decoder for decoding received turbo encoded data, such as LTE channel coded data. As described below, a turbo decoder comprises at least two soft decision decoders that are serially coupled: "A Turbo decoder consists of two single soft-in soft-out (SISO) decoders, which work iteratively. The output of the first (upper decoder) feeds into the second to form a Turbo decoding iteration. Interleaver and deinterleaver blocks re-order data in this process." *See* ALTERA CORP., 3GPP LTE TURBO REFERENCE DESIGN, 7 (Jan. 2011), *available at* https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an505.pdf. An example turbo decoder is shown below. The labeled "1st constituent decoder" and "2nd constituent decoder" are soft decision decoders that are adapted to receive data associated with corresponding data paths, as shown at least by the labeled "soft data," "soft parity 1, ptail 1," and "soft parity 2, ptail 2," data being input into the 1st constituent decoder and 2nd constituent decoder:

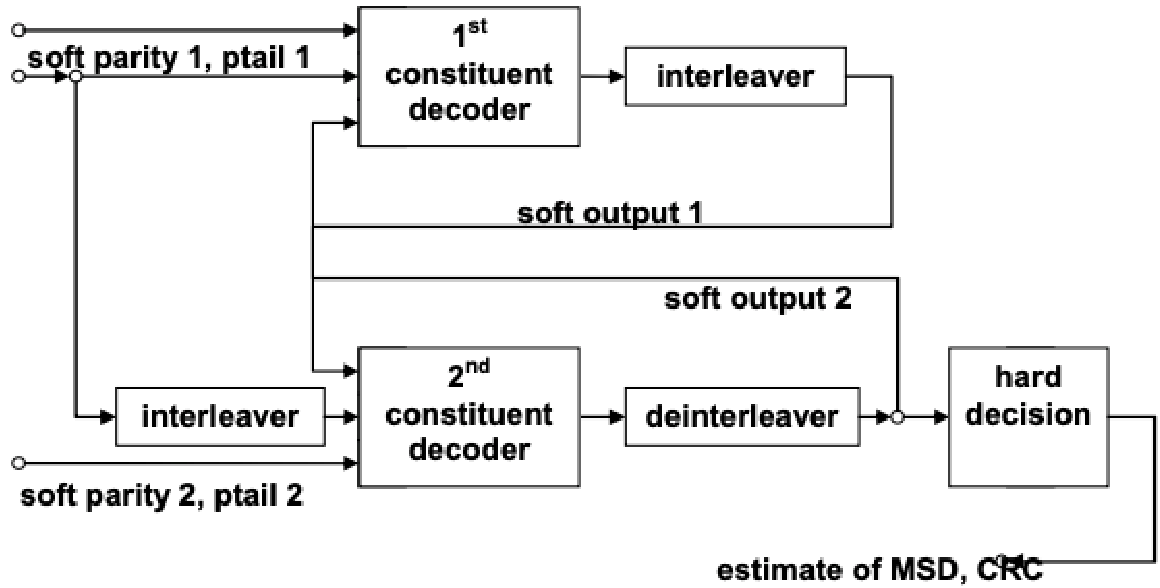


Figure 18: Turbo decoder

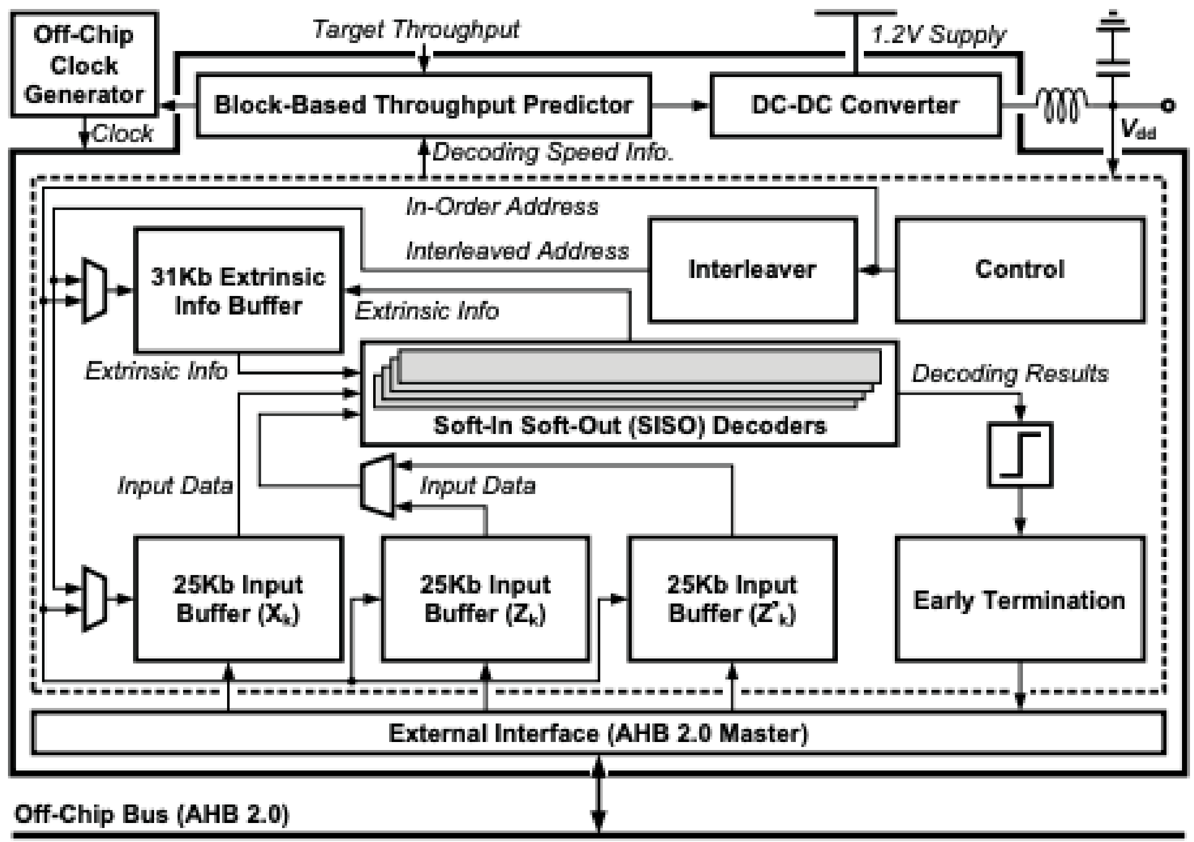
See

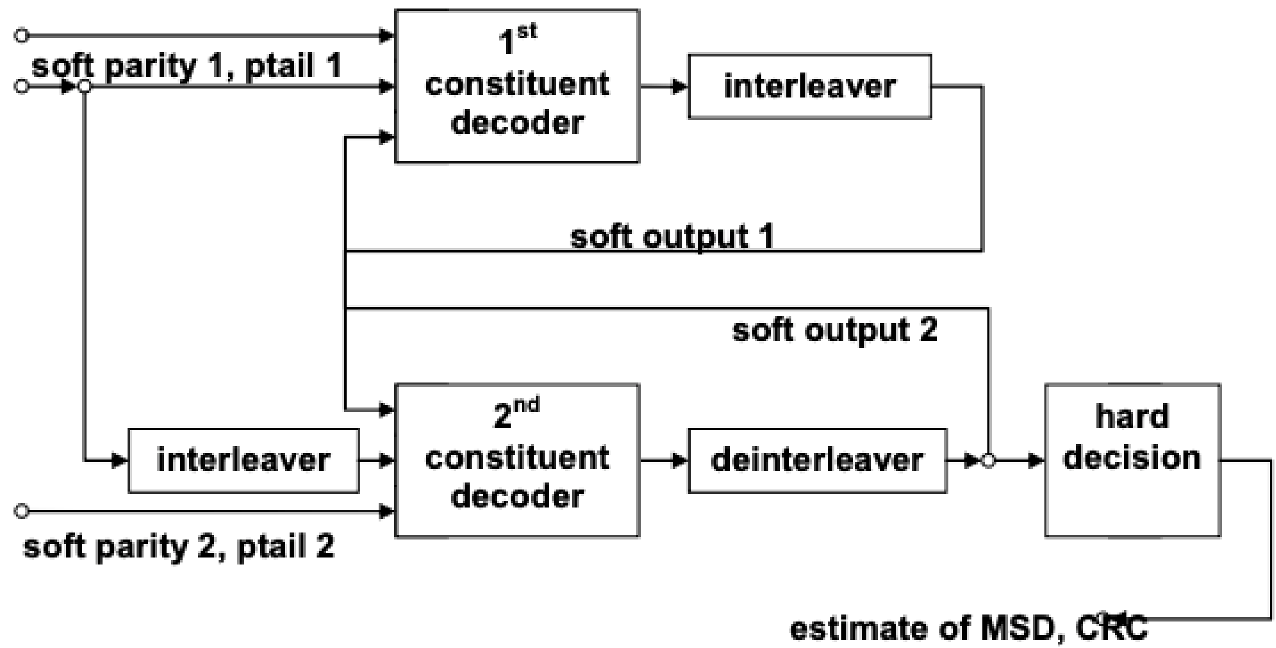
See, e.g., 3GPP TS 26.267, at 25.

As shown in the example figure, decoding occurs from the first soft decision decoder, "1st constituent decoder," to the second, or last, soft decision decoder, "2nd constituent decoder." The first soft decision decoder outputs "soft output 1." This "soft output 1" is fed as input into the second soft decision decoder. The second soft decision decoder is the last soft decision decoder, which is adapted to output data for the serially coupled series of soft decision decoders, labeled as "estimate of MSD, CRC" in the figure.

See also Cheng et. al. "A 0.077 to 0.168 nj/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine," 2010 IEEE Custom Integrated Circuits Conference (CICC) (19-22 Sept. 2010), at 3, *available at* https://dspace.mit.edu/bitstream/handle/1721.1/72198/Chandrakasan-a%200.077%20to%200.168.pdf?sequence=1&isAllowed=y:

	"Figure 3 shows the system architecture. The blocks in the dashed box handle the turbo decoding operations, and those outside the dashed box belong to the DVFS scheme. Turbo decoding is an iterative process with several turbo iterations. Each turbo iteration comprises two soft-in, soft-out (SISO) decoding processes using BCJR algorithm [8]with the first one performed on the input code block in the original order and the second one in an order generated by the interleaver block." *See also id.* at Fig. 3:

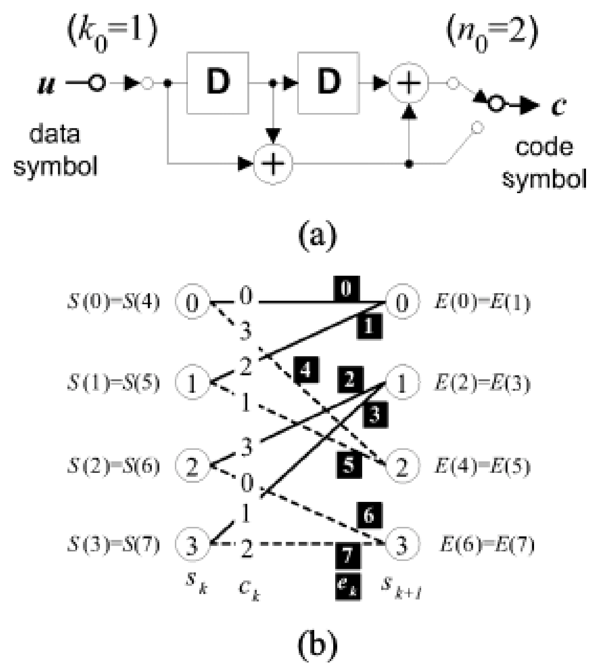
	 Fig. 3. The system architecture.
at least one memory module that is electrically coupled to an output of a	The ’295 Accused Instrumentalities provide at least one memory module that is electrically coupled to an output of a corresponding soft decision decoder, wherein the output of the memory module associated with the last soft decision decoder is fed back as an input to the first soft decision decoder of

corresponding soft decision decoder, wherein the output of the memory module associated with the last soft decision decoder is fed back as an input to the first soft decision decoder of each of the at least one decoders.	each of the at least one decoders. For example, the representative product, ZenFone 7 Pro, includes at least one memory module (e.g., “interleaver” to the right of the “1st constituent decoder” and “deinterleaver” in the figure, that is electrically coupled to an output of a corresponding soft decision decoder (e.g., “1st constituent decoder” and “2nd constituent decoder”)), wherein the output of the memory module associated with the last soft decision decoder (“deinterleaver”) is fed back as an input to the first soft decision decoder of each of the at least one decoders, as shown below:  **Figure 18: Turbo decoder** *See, e.g.*, 3GPP TS 26.267, at 25. In the example, the “deinterleaver” memory module is associated with the second, or last, soft decision decoder, “2nd constituent decoder.” The output of the deinterleaver, “soft output 2,” is fed back as an

	input to the first soft decision decoder, "1st constituent decoder" of the turbo decoder. Additional evidence that the "interleaver" and "deinterleaver" comprising memory modules is shown in source code associated with the figure:

```
/* initialize memory */
 Le12 = (IntLLR*)&decBits[0];
 Le21 = (IntLLR*)&decBits[sizeof(IntLLR)*(NRB_INFO_CRC + NRB_TAIL)];

 memset(Le12, 0, sizeof(IntLLR)*(NRB_INFO_CRC + NRB_TAIL));
 memset(Le21, 0, sizeof(IntLLR)*(NRB_INFO_CRC + NRB_TAIL));

 /* iterative decoding */
 for (i = 0; i < FEC_ITERATIONS; i++) {
   memcpy(Le12, Le21, sizeof(IntLLR)*(NRB_INFO_CRC + NRB_TAIL));

   /* add received systematic bits to extrinsic information */
   for (j = 0; j < NRB_INFO_CRC+NRB_TAIL; j++) {
     temp = (Int32)Le12[j] + (Int32)syst1[j];
     Le12[j] = (ABS(temp) < LLR_MAX) ?
       (IntLLR)temp : (IntLLR)(SIGN(temp)*LLR_MAX);
   }
   /* decode code one (produces Le12) */
   Bcjr(parity1, Le12);

   /* interleave extrinsic information (produces interleaved Le12) */
   Interleave(Le12, Le21);

   /* add received systematic bits to extrinsic information */
   for (j = 0; j < NRB_INFO_CRC; j++) {
     temp = (Int32)Le21[j] + (Int32)syst1[interleaverSeq[j]];
     Le21[j] = (ABS(temp) < LLR_MAX) ?
       (IntLLR)temp : (IntLLR)((SIGN(temp))*LLR_MAX);
```

	} *for (j = 0; j < NRB_TAIL; j++) {* *Le21[j+NRB_INFO_CRC] = syst2[j];* *}* */* decode code two (produces interleaved Le21) */* *Bcjr(parity2, Le21);* */* deinterleave extrinsic information (produces Le21) */* *Deinterleave(Le21);* *}* *See* "Digital cellular telecommunications system (Phase 2+); Universal Mobile Telecommunications System (UMTS); eCall data transfer; In-band modem solution; ANSI-C reference code (3GPP TS 26.268 version 11.0.0 Release 11)," at 21, ecall-fec.c lines 232-268, *available at* https://www.etsi.org/deliver/etsi_ts/126200_126299/126268/11.00.00_60/ts_126268v110000p.pdf. *See also* Valenti et al., "UMTS Turbo Code and an Efficient Decoder," International Journal of Wireless Information Networks, Vol. 8, No. 4 (Oct. 2001), at 207, *available at* https://community.wvu.edu/~mcvalenti/documents/valenti01.pdf "Two key observations should be pointed out before going into the details of the algorithm: (1) It does not matter whether the forward sweep or the reverse sweep is performed first; and (2) while the partial path metrics for the entire first sweep (forward or backward) must be stored in memory, they do not need to be stored for the entire second sweep. This is because the LLR values can be computed during the second sweep, and thus partial path metrics for only two stages of the trellis (the current and previous stages) must be maintained during the second sweep." *See also* Mansour et al., "VLSI Architectures for SISO-APP Decoders," IEEE Transactions On Very Large Scale Integration ("VLSI") Systems, Vol. 11, No. 4 (Aug. 2003): "Fig. 1. A (2, 1, 3) convolutional code. (a) An encoder with 2 memory delay elements (D) and modulo 2 adders, data symbol alphabet {0, 1}, code symbol alphabet {0, 1, 2, 3}, memory states {0, 1, 2, 3}, and code rate R = (1=2). (b) A trellis section where solid edges correspond to u = 0, and dashed edges

	correspond to u = 1. The output code symbols c are shown on the edges. The edges are numbered with black squares, and the edge starting and ending states are shown on the left and right, respectively.” *See also id.* at FIG. 1: 

Caveat: The notes and/or cited excerpts utilized herein are set forth for illustrative purposes only and are not meant to be limiting in any manner. For example, the notes and/or cited excerpts, may or may not be supplemented or substituted with different excerpt(s) of the relevant reference(s), as appropriate. Further, to the extent any error(s) and/or omission(s) exist herein, all rights are reserved to correct the same.